

Appl. No. : 10/615,326  
Filed : July 7, 2003

## AMENDMENTS TO THE CLAIMS

Claims 1-11 and 13-21 are pending in this application. Claims 1-11 and 13-21 remain as previously pending.

1. (Previously Presented) A method of making a memory module comprising:

attaching at least one memory integrated circuit to a printed circuit board, said printed circuit board comprising data bus contacts on a portion thereof;

coupling said data bus contacts on said printed circuit board to data bus terminals on said memory integrated circuit through a bus switch; and

interfacing a state decoder with a memory controller, wherein said state decoder selectively controls said bus switch to reduce data bus capacitance.

2. (Original) The method of Claim 1, wherein the memory integrated circuit comprises synchronous DRAM.

3. (Previously Presented) The method of Claim 1, further comprising interfacing the state decoder with the bus switch.

4. (Previously Presented) The method of Claim 1, wherein the state decoder is structured to decode at least one control gate and control the bus switch in response thereto.

5. (Previously Presented) A method of making a memory module comprising:

attaching at least one memory integrated circuit to a printed circuit board, said printed circuit board comprising data bus contacts on a portion thereof; and

coupling said data bus contacts on said printed circuit board to data bus terminals on said memory integrated circuit;

positioning a bus switch in a data path to the memory integrated circuit; and

interfacing a state decoder with a memory controller, wherein said state decoder selectively controls said bus switch to reduce data bus capacitance.

6. (Previously Presented) The method of Claim 5, wherein the memory integrated circuit comprises synchronous DRAM.

7. (Previously Presented) The method of Claim 5, further comprising interfacing the state decoder with the bus switch.

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8. (Previously Presented) The method of Claim 5, wherein the state decoder is structured to decode at least one control gate and control the bus switch in response thereto.

9. (Previously Presented) The method of Claim 5, wherein the memory integrated circuit comprises the bus switch.

10. (Original) The method of Claim 5, wherein the bus switch is positioned externally with respect to the memory integrated circuit.

11. (Previously Presented) A method of making a memory integrated circuit comprising the acts of:

connecting data input terminals to an input portion of a bus switch;  
connecting an output portion of said bus switch to a data input buffer;  
coupling an output of said data input buffer to a memory storage circuit;  
and

connecting a state decoder to a memory controller, wherein said state decoder selectively controls said bus switch to reduce data bus capacitance.

12. (Canceled)

13. (Previously Presented) The method of Claim 1 wherein the bus switch electrically removes a portion of the data bus associated with unaccessed memory circuits.

14. (Previously Presented) The method of Claim 13 wherein capacitance of unaccessed memory circuits is associated with the portion of the data bus.

15. (Previously Presented) The method of Claim 1 wherein the memory integrated circuit comprises the bus switch.

16. (Previously Presented) The method of Claim 1 wherein the memory integrated circuit comprises the state decoder.

17. (Previously Presented) The method of Claim 5 wherein the memory integrated circuit comprises the state decoder.

18. (Previously Presented) The method of Claim 11 wherein the state decoder is located within the memory integrated circuit.

19. (Previously Presented) The method of Claim 11 wherein the bus switch is located within the memory integrated circuit.

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20. (Previously Presented) The method of Claim 11, further comprising interfacing the state decoder with the bus switch.

21. (Previously Presented) The method of Claim 11, wherein the state decoder is structured to decode at least one control gate and control the bus switch in response thereto.